ARGUMENTS

Claim Rejections

Claims 1, 3-4 and 9-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ahn in view of Kaneko.

Response:

Ahn's disclosure as cited by the Examiner, (C 1, L 64 – 67) indicates that Ahn intended for more than a single common area to exist. Note, column 1, lines 64 66, "...same interrupt routines are stored in the same regions of the memory banks when an interrupt occurs..." Furthermore, Ahn indicates that only some of the similar routines will be stored in a same common area. It is obvious from this disclosure that Ahn teaches managing external memory using address translation and utilizes a collection of common areas of memory.

Regarding Kaneko's bank switching scheme, bank switching programs are stored in a plurality of memory banks (bank A and bank B) respectively and an interrupt handling subroutine is stored in a specific bank (Fig.7; column 11, lines 11-25). When an interrupt occurs during the execution of the main routine in the memory bank B, the bank switching program of bank B switches the execution to bank A, and then the bank switching program of bank A loads the start address Y of the interrupt handling subroutine. Next, the CPU directly executes the interrupt handling subroutine according to the address Y (Fig. 7; column 11, line 60 to column 12, line 13). In other words, Kaneko's bank switching scheme uses bank switching programs to control switching between different memory banks and directly informs the CPU of the start address Y of the interrupt handling subroutine for processing the interrupt. Therefore, when an interrupt occurs during the execution of the main routine in a specific memory block, the CPU does not attempt to access an interrupt routine stored in the same specific memory block for handling the interrupt. Instead, the CPU is directly directed to another memory bank containing the desired interrupt routine through the prior art bank

switching scheme taught by Kaneko.

As mentioned above, **since the CPU does not issue a memory address for accessing an interrupt routine stored in the same specific memory block for handling the interrupt, Kaneko's bank switching scheme does not translate the memory address to another memory address to which the desired interrupt routine corresponds.** In short, according to Kaneko's disclosure, the CPU does not regard each bank as one bank having an interrupt routine, and no memory address mapping is needed. Compared with Kaneko's bank switching scheme, the CPU of the present invention, however, regards each bank (i.e., page) as one bank (i.e., page) having an interrupt routine logically. Therefore, as disclosed in paragraph [0020] of the specification, after receiving a memory address for accessing a common area (e.g., an interrupt routine) in a specific memory bank where an interrupt occurs when the specific memory bank is currently selected, a claimed address translator maps the memory address to one common area shared by all banks (i.e., pages).

Briefly summarized, Kaneko teaches storing an interrupt routine in a single common area of the external memory (Figs.7, 8, 10, and 11), however, Kaneko fails to teach or suggest controlling the CPU to firstly access a common area of a specific page in an external memory logically using a memory address, and then mapping the virtual common area in the specific page pointed to by the memory address to a common area of the external memory. Therefore, the claimed feature "**a common area of each page pointed to by the microprocessor** being mapped to one common area of the external memory" is neither taught nor suggested by Ahn in view of Kaneko.

Applicants believe that independent claims 1 and 9 are placed in a condition for allowance over Ahn in view of Kaneko. Claims 3 and 4 are dependent on claim 1 and claims 10-11 are dependent on claim 9 and should be allowable if claims 1 and 9 are found allowable. Applicants respectfully request that the Examiner reconsider claims 1, 3-4, and 9-11 in light of Applicant's arguments above.

Claims 5-6 and 12-13 are rejected under U.S.C. 103 (a) as being unpatentable over Ahn and Kaneko in view of Applicant's submitted prior art Intel Application Note Migration from the MCS 51 Microcontroller to the MCS 251 Microcontroller.

Response:

Claims 5-6 and 12-13 are dependent upon claims 1 and 9 respectively, and should be allowed if claims 1 and 9 are found allowable. Reconsideration of claims 5-6 and 12-13 is respectfully requested.

Claims 7 and 14 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ahn and Kaneko.

Response:

Both Ahn and Kaneko fail to teach or suggest applying the bank switching to a flash memory. In other words, no cited reference/prior art is provided to support that it is obvious to one of average skill in the art to apply the bank switching to a flash memory.

In addition, claims 7 and 14 are dependent upon claims 1 and 9 respectively, and should be allowed if claims 1 and 9 are found allowable. Reconsideration of claims 7 and 14 is respectfully requested.

Applicants respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)